# EAST Search History

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| L1 | 638 | dataline | US-PGPUB; USPAT; USOCR; EPO; JPO | OR | ON | 2006/08/29 13:34 |
| L2 | 92851 | data adj line | US-PGPUB; USPAT; USOCR; EPO; JPO | OR | ON | 2006/08/29 13:34 |
| L3 | 93066 | 1 or 2 | US-PGPUB; USPAT; USOCR; EPO; JPO | OR | ON | 2006/08/29 13:34 |
| L4 | 1980611 | driver or driving | US-PGPUB; USPAT; USOCR; EPO; JPO | OR | ON | 2006/08/29 13:34 |
| L5 | 2400 | 3 adj 4 | US-PGPUB; USPAT; USOCR; EPO; JPO | OR | ON | 2006/08/29 13:34 |
| L6 | 722139 | segment | US-PGPUB; USPAT; USOCR; EPO; JPO | OR | ON | 2006/08/29 13:35 |
| L7 | 24 | 5 same 6 | US-PGPUB; USPAT; USOCR; EPO; JPO | OR | ON | 2006/08/29 13:35 |
| L8 | 8 | vadi-vasisht-mantra.in. | US-PGPUB; USPAT; USOCR; EPO; JPO | OR | ON | 2006/08/29 13:35 |
| L9 | 39 | schultz-david-p$.in. | US-PGPUB; USPAT; USOCR; EPO; JPO | OR | ON | 2006/08/29 13:35 |
| L10 | 143 | young-steven-p$.in. | US-PGPUB; USPAT; USOCR; EPO; JPO | OR | ON | 2006/08/29 13:36 |

Day : Tuesday
Date: 8/29/2006

PALM INTRANET

Time: 13:41:30

## Inventor Name Search Result

Your Search was:

Last Name = VADI
First Name = VASISHT

| Application# | Patent# | Status | Date Filed | Title | Inventor Name |
|---|---|---|---|---|---|
| 10090250 | Not Issued | 61 | 03/01/2002 | High speed configurable transceiver architecture | VADI, VASISHT M. |
| 10453235 | 6975145 | 150 | 06/02/2003 | GLITCHLESS DYNAMIC MULTIPLEXER WITH SYNCHRONOUS AND ASYNCHRONOUS CONTROLS | VADI, VASISHT M. |
| 10806697 | Not Issued | 95 | 03/22/2004 | DATA MONITORING FOR SINGLE EVENT UPSET IN A PROGRAMMABLE LOGIC DEVICE | VADI, VASISHT M. |
| 10090239 | 6911842 | 150 | 03/01/2002 | LOW JITTER CLOCK FOR A PHYSICAL MEDIA ACCESS SUBLAYER ON A FIELD PROGRAMMABLE GATE ARRAY | VADI, VASISHT M. |
| 10796750 | Not Issued | 71 | 03/08/2004 | SEGMENTED DATALINE SCHEME IN A MEMORY WITH ENHANCED FULL FAULT COVERAGE MEMORY CELL TESTABILITY | VADI, VASISHT MANTRA |
| 10836722 | Not Issued | 95 | 04/30/2004 | DIFFERENTIAL CLOCK TREE IN AN INTEGRATED CIRCUIT | VADI, VASISHT MANTRA |
| 10836841 | Not Issued | 93 | 04/30/2004 | RECONFIGURATION PORT FOR DYNAMIC RECONFIGURATION - SUB-FRAME ACCESS FOR RECONFIGURATION | VADI, VASISHT MANTRA |
| 10836960 | Not Issued | 95 | 04/30/2004 | RECONFIGURATION PORT FOR DYNAMIC RECONFIGURATION-CONTROLLER | VADI, VASISHT MANTRA |
| 10836961 | Not Issued | 89 | 04/30/2004 | Reconfiguration port for dynamic reconfiguration-system monitor interface | VADI, VASISHT MANTRA |

| | | | | | |
|---|---|---|---|---|---|
| 10837009 | Not Issued | 95 | 04/30/2004 | PROGRAMMABLE LOGIC DEVICE HAVING AN EMBEDDED DIFFERENTIAL CLOCK TREE | VADI, VASISHT MANTRA |
| 10837329 | 7071756 | 150 | 04/30/2004 | CLOCK MULTIPLEXING SYSTEM | VADI, VASISHT MANTRA |
| 10837331 | Not Issued | 30 | 04/30/2004 | Reconfiguration port for dynamic reconfiguration | VADI, VASISHT MANTRA |
| 10970964 | Not Issued | 30 | 10/22/2004 | Method and system for configuring an integrated circuit | VADI, VASISHT MANTRA |
| 10971394 | Not Issued | 41 | 10/22/2004 | Method and apparatus for a multiplexed address line driver | VADI, VASISHT MANTRA |
| 11055475 | Not Issued | 30 | 02/10/2005 | Bidirectional register segmented data busing | VADI, VASISHT MANTRA |
| 11059967 | Not Issued | 71 | 02/17/2005 | Efficient implementation of a bypassable flip-flop with a clock enable | VADI, VASISHT MANTRA |
| 11083812 | Not Issued | 30 | 03/18/2005 | Adjustable global tap voltage to improve memory cell yield | VADI, VASISHT MANTRA |
| 11408364 | Not Issued | 20 | 04/21/2006 | Digital signal processing element having an arithmetic logic unit | VADI, VASISHT MANTRA |
| 11432823 | Not Issued | 20 | 05/12/2006 | Digital signal processing circuit having input register blocks | VADI, VASISHT MANTRA |
| 11432846 | Not Issued | 20 | 05/12/2006 | Digital signal processing circuit having a pattern detector circuit | VADI, VASISHT MANTRA |
| 11432847 | Not Issued | 20 | 05/12/2006 | Digital signal processing circuit having a pattern detector circuit for convergent rounding | VADI, VASISHT MANTRA |
| 11432848 | Not Issued | 20 | 05/12/2006 | Digital signal processing circuit having a pre-adder circuit | VADI, VASISHT MANTRA |
| 11433120 | Not Issued | 20 | 05/12/2006 | Digital signal processing block having a wide multiplexer | VADI, VASISHT MANTRA |
| 11433331 | Not Issued | 19 | 05/12/2006 | Digital signal processing circuit having a SIMD circuit | VADI, VASISHT MANTRA |
| 11433332 | Not Issued | 19 | 05/12/2006 | Digital signal processing circuit having a pattern circuit for determining termination conditions | VADI, VASISHT MANTRA |
| 11433369 | Not Issued | 20 | 05/12/2006 | Architectural floorplan for a digital signal processing circuit | VADI, VASISHT MANTRA |
| 11433517 | Not Issued | 20 | 05/12/2006 | Digital signal processing circuit having an adder circuit with carry-outs | VADI, VASISHT MANTRA |
| 11445066 | Not | 30 | 05/31/2006 | Pipeline FFT architecture for a | VADI, VASISHT |

| | | | | | |
|---|---|---|---|---|---|
| | Issued | | | programmable logic device | MANTRA |
| 11433333 | Not Issued | 20 | 05/12/2006 | Arithmetic logic unit circuit | VADI, VASISHT MANTRA |

# Inventor Search Completed: No Records to Display.

**Search Another: Inventor** **Last Name** vadi **First Name** vasisht Search

To go back use Back button on your browser toolbar.

Back to PALM | ASSIGNMENT | OASIS | Home page

Day : Tuesday
Date: 8/29/2006

PALM INTRANET

Time: 13:45:23

## Inventor Name Search Result

Your Search was:

Last Name = SCHULTZ
First Name = DAVID

| Application# | Patent# | Status | Date Filed | Title | Inventor Name |
|---|---|---|---|---|---|
| 60192716 | Not Issued | 159 | 03/28/2000 | Backpack with audio player | SCHULTZ, DAVID EVAN |
| 29116532 | D451506 | 150 | 01/04/2000 | USER OPERATABLE DIGITAL DEVICE | SCHULTZ, DAVID EVAN |
| 09154416 | 6361499 | 150 | 09/16/1998 | MULTIPLE ANGLE NEEDLE GUIDE | SCHULTZ, DAVID F. |
| 60002014 | Not Issued | 159 | 08/08/1995 | ELECTRONIC ENGINE CONTROL SYSTEM HAVING THROTTLE ADVANCE CIRCUIT | SCHULTZ, DAVID F. |
| 07149691 | 4951925 | 150 | 01/28/1988 | FENCE CONNECTOR ASSEMBLY | SCHULTZ, DAVID H. |
| 07212417 | Not Issued | 161 | 06/27/1988 | FISHING LURE RETAINER | SCHULTZ, DAVID H. |
| 07233830 | 4982933 | 150 | 08/19/1988 | FENCE CONNECTOR CLIP AND ASSEMBLY | SCHULTZ, DAVID H. |
| 07520275 | 4986513 | 150 | 05/07/1990 | FENCE CONNECTOR ASSEMBLY | SCHULTZ, DAVID H. |
| 10355715 | Not Issued | 89 | 01/31/2003 | Support for network interface devices | SCHULTZ, DAVID J. |
| 10355789 | Not Issued | 161 | 01/31/2003 | Rehabilitation kit for closures | SCHULTZ, DAVID J. |
| 11199578 | Not Issued | 30 | 08/08/2005 | Apparatus and method of dispensing fluid | SCHULTZ, DAVID J. |
| 11199587 | Not Issued | 30 | 08/08/2005 | Apparatus and method of dispensing fluid | SCHULTZ, DAVID J. |
| 29213102 | Not Issued | 94 | 09/13/2004 | LID WITH VARIABLE INNER ORIFICE | SCHULTZ, DAVID J. |
| 60623867 | Not Issued | 159 | 11/02/2004 | Proportional fill dispenser | SCHULTZ, DAVID J. |
| 06838057 | Not Issued | 161 | 02/28/1986 | TRIGGER GUARD | SCHULTZ, DAVID J. |

| | | | | | |
|---|---|---|---|---|---|
| 60748986 | Not Issued | 20 | 12/09/2005 | Sanitary lid dispenser | SCHULTZ, DAVID JOHN |
| 06709437 | Not Issued | 161 | 05/01/1985 | TRIGGER GUARD | SCHULTZ, DAVID L. |
| 08895976 | 5988397 | 150 | 07/17/1997 | SCREEN FOR VIBRATORY SEPERATOR | SCHULTZ, DAVID L. |
| 09492560 | 6353334 | 150 | 01/27/2000 | Circuit for converting a logic signal on an output node to a pair of low-voltage differential signals | SCHULTZ, DAVID P. |
| 09546305 | 6323681 | 150 | 04/10/2000 | Circuits and methods for operating a multiplexer array | SCHULTZ, DAVID P. |
| 09684539 | 6445245 | 150 | 10/06/2000 | DIGITALLY CONTROLLED IMPEDANCE FOR I/O OF AN INTEGRATED CIRCUIT DEVICE | SCHULTZ, DAVID P. |
| 09858732 | Not Issued | 161 | 05/15/2001 | Microprocessor with programmable logic in the data path | SCHULTZ, DAVID P. |
| 09865813 | 6429682 | 150 | 05/25/2001 | CONFIGURATION BUS INTERFACE CIRCUIT FOR FPGAS | SCHULTZ, DAVID P. |
| 10007167 | 6489837 | 150 | 11/30/2001 | DIGITALLY CONTROLLED IMPEDANCE FOR I/O OF AN INTEGRATED CIRCUIT DEVICE | SCHULTZ, DAVID P. |
| 10043769 | 6781407 | 150 | 01/09/2002 | FPGA AND EMBEDDED CIRCUITRY INITIALIZATION AND PROCESSING | SCHULTZ, DAVID P. |
| 10086129 | Not Issued | 95 | 02/28/2002 | METHOD AND SYSTEM FOR FLEXIBLY NESTING JTAG TAP CONTROLLERS FOR FPGA-BASED SYSTEM-ON-CHIP (SOC) | SCHULTZ, DAVID P. |
| 10136141 | 6525562 | 150 | 04/30/2002 | PROGRAMMABLE LOGIC DEVICE CAPABLE OF PRESERVING STATE DATA DURING PARTIAL OR COMPLETE RECONFIGURATION | SCHULTZ, DAVID P. |
| 10736161 | Not Issued | 71 | 12/15/2003 | Two-stage pressure relief valve | SCHULTZ, DAVID P. |
| 10796750 | Not Issued | 71 | 03/08/2004 | SEGMENTED DATALINE SCHEME IN A MEMORY WITH ENHANCED FULL FAULT COVERAGE MEMORY CELL TESTABILITY | SCHULTZ, DAVID P. |

| | | | | | |
|---|---|---|---|---|---|
| 10806697 | Not Issued | 95 | 03/22/2004 | DATA MONITORING FOR SINGLE EVENT UPSET IN A PROGRAMMABLE LOGIC DEVICE | SCHULTZ, DAVID P. |
| 10836841 | Not Issued | 93 | 04/30/2004 | RECONFIGURATION PORT FOR DYNAMIC RECONFIGURATION - SUB-FRAME ACCESS FOR RECONFIGURATION | SCHULTZ, DAVID P. |
| 10836960 | Not Issued | 95 | 04/30/2004 | RECONFIGURATION PORT FOR DYNAMIC RECONFIGURATION-CONTROLLER | SCHULTZ, DAVID P. |
| 10836961 | Not Issued | 89 | 04/30/2004 | Reconfiguration port for dynamic reconfiguration-system monitor interface | SCHULTZ, DAVID P. |
| 10837171 | 7102555 | 150 | 04/30/2004 | BOUNDARY-SCAN CIRCUIT USED FOR ANALOG AND DIGITAL TESTING OF AN INTEGRATED CIRCUIT | SCHULTZ, DAVID P. |
| 10837331 | Not Issued | 30 | 04/30/2004 | Reconfiguration port for dynamic reconfiguration | SCHULTZ, DAVID P. |
| 10898582 | Not Issued | 41 | 07/23/2004 | Programmable gate array and embedded circuitry initialization and processing | SCHULTZ, DAVID P. |
| 10970964 | Not Issued | 30 | 10/22/2004 | Method and system for configuring an integrated circuit | SCHULTZ, DAVID P. |
| 10971220 | Not Issued | 30 | 10/22/2004 | Error checking parity and syndrome of a block of data with relocated parity bits | SCHULTZ, DAVID P. |
| 10971394 | Not Issued | 41 | 10/22/2004 | Method and apparatus for a multiplexed address line driver | SCHULTZ, DAVID P. |
| 11135979 | Not Issued | 20 | 05/24/2005 | Error correction for multiple word read | SCHULTZ, DAVID P. |
| 11408364 | Not Issued | 20 | 04/21/2006 | Digital signal processing element having an arithmetic logic unit | SCHULTZ, DAVID P. |
| 11433333 | Not Issued | 20 | 05/12/2006 | Arithmetic logic unit circuit | SCHULTZ, DAVID P. |
| 11449172 | Not Issued | 25 | 06/08/2006 | Methods of selectively programming programmable integrated circuits to compensate for process variations and/or mask revisions | SCHULTZ, DAVID P. |
| 11449240 | Not Issued | 30 | 06/08/2006 | Programmable integrated circuit with selective programming to | SCHULTZ, DAVID P. |

| | | | | | |
|---|---|---|---|---|---|
| | | | | compensate for process variations and/or mask revisions | |
| 29187178 | D494450 | 150 | 07/29/2003 | HYDRAULIC HOSE PAIR GROMMET | SCHULTZ, DAVID P. |
| 60381184 | Not Issued | 159 | 05/16/2002 | Integrated three function valve | SCHULTZ, DAVID P. |
| 60589887 | Not Issued | 159 | 07/20/2004 | Error checking parity and syndrome of a block of data with relocated parity bits | SCHULTZ, DAVID P. |
| 08072295 | Not Issued | 161 | 06/04/1993 | LOW CURRENT OPTIONAL INVERTER | SCHULTZ, DAVID P. |
| 08194552 | Not Issued | 166 | 02/10/1994 | LOW CURRENT POWER-ON RESET CIRCUIT WITH HIGH THRESHOLD INVERTER AND LOW CURRENT SOURCE | SCHULTZ, DAVID P. |
| 08204939 | 5399924 | 150 | 03/01/1994 | LOW CURRENT OPTIONAL INVERTER | SCHULTZ, DAVID P. |

Search and Display More Records.

**Search Another: Inventor** **Last Name** schultz **First Name** david Search

To go back use Back button on your browser toolbar.

Back to PALM | ASSIGNMENT | OASIS | Home page

Day : Tuesday
Date: 8/29/2006

PALM INTRANET

Time: 13:46:52

## Inventor Name Search Result

Your Search was:

Last Name = YOUNG
First Name = STEVEN

| Application# | Patent# | Status | Date Filed | Title | Inventor Name |
|---|---|---|---|---|---|
| 09563779 | 6429698 | 150 | 05/02/2000 | CLOCK MULTIPLEXER CIRCUIT WITH GLITCHLESS SWITCHING | YOUNG, STEVEN P. |
| 09565431 | 6373279 | 150 | 05/05/2000 | FPGA lookup table with dual ended writes for ram and shift register modes | YOUNG, STEVEN P. |
| 09566052 | 6529040 | 150 | 05/05/2000 | FPGA LOOKUP TABLE WITH SPEED READ DECODER | YOUNG, STEVEN P. |
| 09566398 | 6445209 | 150 | 05/05/2000 | FPGA LOOKUP TABLE WITH NOR GATE WRITE DECODER AND HIGH SPEED READ DECODER | YOUNG, STEVEN P. |
| 09569745 | 6204691 | 150 | 05/11/2000 | FPGA with a plurality of input reference voltage levels grouped into sets | YOUNG, STEVEN P. |
| 09574115 | 6288568 | 150 | 05/19/2000 | FPGA architecture with deep look-up table rams | YOUNG, STEVEN P. |
| 09574300 | 6373779 | 150 | 05/19/2000 | Block RAM having multiple configurable write modes for use in a field programmable gate array | YOUNG, STEVEN P. |
| 09574445 | 6297665 | 150 | 05/19/2000 | FPGA architecture with dual-port deep look-up table RAMS | YOUNG, STEVEN P. |
| 09574534 | 6323682 | 150 | 05/19/2000 | FPGA architecture with wide function multiplexers | YOUNG, STEVEN P. |
| 09574714 | 6362650 | 150 | 05/18/2000 | Method and apparatus for incorporating a multiplier into an FPGA | YOUNG, STEVEN P. |
| 09574741 | 6204690 | 150 | 05/18/2000 | FPGA architecture with offset interconnect lines | YOUNG, STEVEN P. |
| 09624515 | 6262597 | 150 | 07/24/2000 | Fifo in FPGA having logic elements that include cascadable shift registers | YOUNG, STEVEN P. |

| | | | | | |
|---|---|---|---|---|---|
| 09624813 | 6493862 | 150 | 07/25/2000 | METHOD FOR COMPRESSING AN FPGA BITSTREAM | YOUNG, STEVEN P. |
| 09624818 | 6526557 | 150 | 07/25/2000 | ARCHITECTURE AND METHOD FOR PARTIALLY RECONFIGURING AN FPGA | YOUNG, STEVEN P. |
| 09625672 | 6282127 | 150 | 07/24/2000 | Block ram with reset to user selected value | YOUNG, STEVEN P. |
| 09680205 | 6346825 | 150 | 10/06/2000 | Block RAM with configurable data width and parity for use in a field programmable gate array | YOUNG, STEVEN P. |
| 09684540 | 6775342 | 150 | 10/06/2000 | DIGITAL PHASE SHIFTER | YOUNG, STEVEN P. |
| 09712038 | 6362648 | 150 | 11/13/2000 | Multiplexer for implementing logic functions in a programmable logic device | YOUNG, STEVEN P. |
| 09757760 | 6522167 | 150 | 01/09/2001 | USER CONFIGURABLE ON-CHIP MEMORY SYSTEM | YOUNG, STEVEN P. |
| 09759051 | 6292022 | 150 | 01/11/2001 | Interconnect structure for a programmable logic device | YOUNG, STEVEN P. |
| 09759432 | 6525565 | 150 | 01/12/2001 | DOUBLE DATA RATE FLIP-FLOP | YOUNG, STEVEN P. |
| 09809675 | 6472909 | 150 | 03/14/2001 | CLOCK ROUTING CIRCUIT WITH FAST GLITCHLESS SWITCHING | YOUNG, STEVEN P. |
| 09920160 | 6612546 | 150 | 08/01/2001 | GATE VALVE WITH DELAYED RETRACTION OF COUNTER PLATE | YOUNG, STEVEN P. |
| 09924356 | 6448809 | 150 | 08/07/2001 | FPGA WITH A PLURALITY OF INPUT REFERENCE VOLTAGE LEVELS | YOUNG, STEVEN P. |
| 09929977 | 6448808 | 150 | 08/15/2001 | INTERCONNECT STRUCTURE FOR A PROGRAMMABLE LOGIC DEVICE | YOUNG, STEVEN P. |
| 09956203 | 6621325 | 150 | 09/18/2001 | STRUCTURES AND METHODS FOR SELECTIVELY APPLYING A WELL BIAS TO PORTIONS OF A PROGRAMMABLE DEVICE | YOUNG, STEVEN P. |
| 09968446 | 6798239 | 150 | 09/28/2001 | PROGRAMMABLE GATE ARRAY HAVING INTERCONNECTING LOGIC TO SUPPORT EMBEDDED FIXED LOGIC CIRCUITRY | YOUNG, STEVEN P. |
| 10008556 | 6603332 | 150 | 11/09/2001 | CONFIGURABLE LOGIC BLOCK FOR PLD WITH LOGIC | YOUNG, STEVEN P. |

| | | | | | |
|---|---|---|---|---|---|
| | | | | GATE FOR COMBINING OUTPUT WITH ANOTHER CONFIGURABLE LOGIC BLOCK | |
| 10043958 | 6573749 | 150 | 01/08/2002 | METHOD AND APPARATUS FOR INCORPORATING A MULTIPLIER INTO AN FPGA | YOUNG, STEVEN P. |
| 10164508 | 6759869 | 150 | 06/05/2002 | LARGE CROSSBAR SWITCH IMPLEMENTED IN FPGA | YOUNG, STEVEN P. |
| 10192354 | 6708191 | 150 | 07/09/2002 | CONFIGURABLE LOGIC BLOCK WITH AND GATE FOR EFFICIENT MULTIPLICATION IN FPGAS | YOUNG, STEVEN P. |
| 10295713 | 6621296 | 150 | 11/15/2002 | FPGA LOOKUP TABLE WITH HIGH SPEED READ DECODER | YOUNG, STEVEN P. |
| 10300212 | 6847228 | 150 | 11/19/2002 | CARRY LOGIC DESIGN HAVING SIMPLIFIED TIMING MODELING FOR A FIELD PROGRAMMABLE GATE ARRAY | YOUNG, STEVEN P. |
| 10342574 | 6777980 | 150 | 01/15/2003 | DOUBLE DATA RATE FLIP-FLOP | YOUNG, STEVEN P. |
| 10354520 | 6768335 | 150 | 01/30/2003 | INTEGRATED CIRCUIT MULTIPLEXER INCLUDING TRANSISTORS OF MORE THAN ONE OXIDE THICKNESS | YOUNG, STEVEN P. |
| 10354587 | 6768338 | 150 | 01/30/2003 | PLD LOOKUP TABLE INCLUDING TRANSISTORS OF MORE THAN ONE OXIDE THICKNESS | YOUNG, STEVEN P. |
| 10376522 | 6798241 | 150 | 02/27/2003 | METHODS FOR ALIGNING DATA AND CLOCK SIGNALS | YOUNG, STEVEN P. |
| 10377461 | 6864715 | 150 | 02/27/2003 | WINDOWING CIRCUIT FOR ALIGNING DATA AND CLOCK SIGNALS | YOUNG, STEVEN P. |
| 10402446 | 6982451 | 150 | 03/27/2003 | SINGLE EVENT UPSET IN SRAM CELLS IN FPGAS WITH HIGH RESISTIVITY GATE STRUCTURES | YOUNG, STEVEN P. |
| 10453235 | 6975145 | 150 | 06/02/2003 | GLITCHLESS DYNAMIC MULTIPLEXER WITH SYNCHRONOUS AND ASYNCHRONOUS CONTROLS | YOUNG, STEVEN P. |
| 10610207 | 7068072 | 150 | 06/30/2003 | INTEGRATED CIRCUIT WITH INTERFACE TILE FOR | YOUNG, STEVEN P. |

| | | | | | |
|---|---|---|---|---|---|
| | | | | COUPLING TO A STACKED-DIE SECOND INTEGRATED CIRCUIT | |
| 10618404 | Not Issued | 93 | 07/11/2003 | COLUMNAR FLOORPLAN | YOUNG, STEVEN P. |
| 10624617 | 6777978 | 150 | 07/21/2003 | STRUCTURES AND METHODS FOR SELECTIVELY APPLYING A WELL BIAS TO PORTIONS OF A PROGRAMMABLE DEVICE | YOUNG, STEVEN P. |
| 10624832 | 7095253 | 150 | 07/21/2003 | PROGRAMMABLE MULTI-CHIP MODULE | YOUNG, STEVEN P. |
| 10683944 | Not Issued | 61 | 10/10/2003 | Columnar architecture | YOUNG, STEVEN P. |
| 10684183 | 6933747 | 150 | 10/10/2003 | STRUCTURES AND METHODS OF TESTING INTERCONNECT STRUCTURES IN PROGRAMMABLE LOGIC DEVICES | YOUNG, STEVEN P. |
| 10742300 | Not Issued | 95 | 12/18/2003 | CHARACTERIZING CIRCUIT PERFORMANCE BY SEPARATING DEVICE AND INTERCONNECT IMPACT ON SIGNAL DELAY | YOUNG, STEVEN P. |
| 10796750 | Not Issued | 71 | 03/08/2004 | SEGMENTED DATALINE SCHEME IN A MEMORY WITH ENHANCED FULL FAULT COVERAGE MEMORY CELL TESTABILITY | YOUNG, STEVEN P. |
| 10836722 | Not Issued | 95 | 04/30/2004 | DIFFERENTIAL CLOCK TREE IN AN INTEGRATED CIRCUIT | YOUNG, STEVEN P. |
| 10837009 | Not Issued | 95 | 04/30/2004 | PROGRAMMABLE LOGIC DEVICE HAVING AN EMBEDDED DIFFERENTIAL CLOCK TREE | YOUNG, STEVEN P. |

Search and Display More Records.

**Search Another: Inventor** **Last Name** young **First Name** steven Search

To go back use Back button on your browser toolbar.

Back to PALM | ASSIGNMENT | OASIS | Home page